Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **N.E**
2. **D0**
3. **N.CC**
4. **Q0**
5. **Q1**
6. **Q2**
7. **Q3**
8. **Q4**
9. **Q5**
10. **NC**
11. **D**
12. **GND**
13. **CP**
14. **N.S**
15. **NC**
16. **Q6**
17. **Q7**
18. **Q8**
19. **Q9**
20. **Q10**
21. **Q11**
22. **NC**
23. **N.Q11**
24. **VCC**

**DIE ID**

**3 2 1 24**

**11 12 13 14**

**23**

**21**

**20**

**19**

**18**

**17**

**16**

**4**

**5**

**6**

**7**

**8**

**9**

**54C905**

**.094”**

**.116”**

**C**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 54C905 C**

**APPROVED BY: DK DIE SIZE .094” X .116” DATE: 2/4/16**

**MFG: NATIONAL THICKNESS .015” P/N: 54C905**

**DG 10.1.2**

#### Rev B, 7/19/02